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				FILE No.
			LIQUID CRYSTAL DISPLAY GROUP	ISSUE OCT. 5.1994
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APPLICABLE DIVISION

■DUTY PANEL DEVELOPMENT
　CENTER

☐TFT DEVELOPMENT CENTER

☐LCD PRODUCTS DEVELOPMENT
　CENTER

☐EL PRODUCTION DEPT.

SPECIFICATION

DEVICE SPECIFICATION for

　Passive Matrix COLOR LCD Unit

　(640×480 dots)

Model No.

LM64C35P

☐CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED
BY _____ *Y. Inoue*

Y. Inoue

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LIQUID CRYSTAL DISPLAY GROUP

SHARP CORPORATION

SHARP

		SPEC No. LC94805A 3	MODEL No. **LM64C35P**
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RECORDS OF REVISION		IDENT. DATA No.	

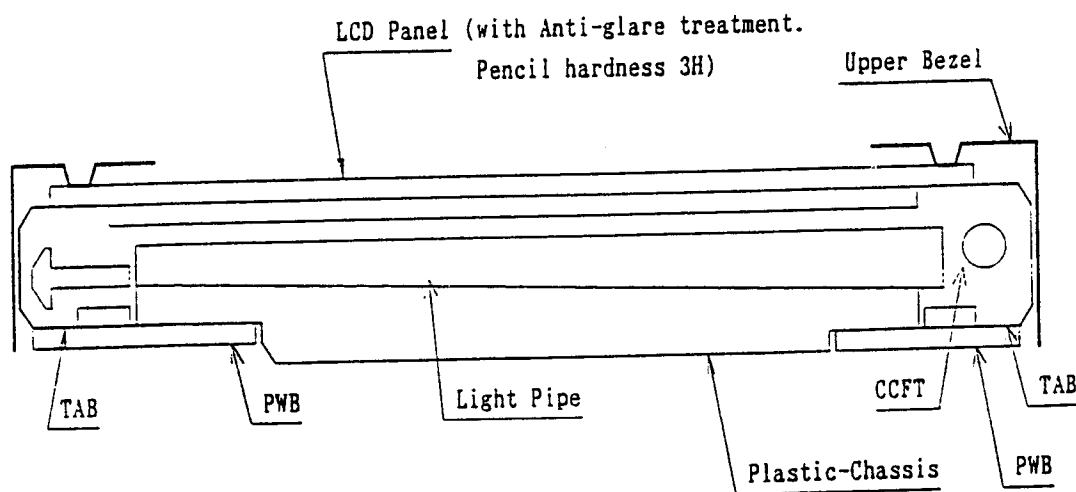| DATE	REF. PAGE PARAGRAPH DRAWING No.	REVISED No.	SUMMARY	CHECK & APPROVAL
OCT. 5.1994	Page 4	△1	D E L E T E D (Input capacitance)	
OCT. 5.1994	Page 1,11,20	△2	R E V I S E D (Table No.)	*Y. Inoue*
OCT. 5.1994	Page 18	△3	R E V I S E D (Characteristics of Backlight)	
Mar.13.1995	Page 22	△4	ADDED	*Y. Inoue*

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1. Application

This data sheet is to introduce the specification of LM64C35P,Passive Matrix type Color LCD Unit.

2. Construction and Outline

Construction: 640×480 dots color display unit consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TAB(tape automated bonding) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically.

Signal ground(VSS) is connected with the metal bezel.

DC/DC converter is built in.

LCD Panel (with Anti-glare treatment. Pencil hardness 3H) / Upper Bezel / TAB / PWB / Light Pipe / CCFT / TAB / Plastic-Chassis / PWB

Outline   : See Fig. 10

Connection : See Fig. 10 and Table 7

3. Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	242.5(W)×179.4(H)×11.5MAX(D)	mm
Effective viewing Area	214.2(W)×161.4(H)	mm
Display format	640(W)×480(H) full dots	—
Dot size	0.085×RGB(W)×0.305(H)	mm
Dot spacing	0.025	mm
*1 Base color	Normally black *2	—
Weight	Approx. 500	g

*1 Due to the characteristics of the LC material, the colors vary
   with environmental temperature.

*2 Negative-type display
   Display data ˇHˇ : ON → transmission
   Display data ˇLˇ : OFF → light isolation

4. Absolute Maximum Ratings
4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	$V_{DD}-V_{SS}$	0	6.0	V	Ta=25 ℃
Input voltage	V_{IN}	-0.3	$V_{DD}+0.3$	V	Ta=25 ℃

4-2 Environmental Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 ℃	+60 ℃	0 ℃	+40 ℃	Note 4)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions (X/Y/Z)
Shock	Note 3)		Note 3)		6 directions (±X±Y±Z)

Note 1) Ta≦40 ℃.....95 % RH Max

Ta＞40 ℃.....Absolute humidity shall be less than Ta=40 ℃/95 % RH.

Note 2)

Table 4

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	－	9.8 m/s²
Vibration width	0.075 mm	－
Interval	10 Hz～500 Hz～10 Hz/11.0 min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X/±Y/±Z

Note 4) Care should be taken so that the LCD Unit may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characterictics

Table 5   Ta=25 °C, V_{DD}=5 V ± 10 %

| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{ss}	Note 1)	4.5	5.0	5.5	V
Contrast adjust voltage	Vcon -Vss	Ta=0 °C	0.8	—	—	V
		Ta=25 °C	1.35	1.95	2.55	V
		Ta=40 °C	—	—	2.80	
Input signal voltage	V_{IN}	"H" level	0.8V_{DD}	V_{DD}	V_{DD}+0.3	V
		"L" level	-0.3	V_{ss}	0.2V_{DD}	V
Input leakage current	I_{IL}	"H" level	—	—	1.0	μA
		"L" level	-1.0	—	—	μA
Supply current (Logic)	I_{DD}	Note 2)	—	160	240	mA
Rush current (Logic)	Irush	Ta=25 °C, Power ON	3 A(pk)×25 ms+1 A(pk)×10 μs max			
Power consumption	Pd	Note 2)	—	800	1 320	mW

Note 1) Under the following conditions.;

    ① Immediately after the rise of DISP signal.   : 3 A×25 ms

    ② Under the situation that DISP signal is on and kept steady.: 1 A×10 μs

Note 2) Under the following conditions.;

    Vcon-Vss : contrast max.(1.95 V TYP)

    V_{DD}-Vss=5 V, Frame frequency=73 Hz, Display pattern = black/white stripe pattern.

Display pattern
```
■■■■■■■■■■■■■■■■■■■■■■■■■
□□□□□□□□□□□□□□□□□□□□□□□□□
■■■■■■■■■■■■■■■■■■■■■■■■■
□□□□□□□□□□□□□□□□□□□□□□□□□
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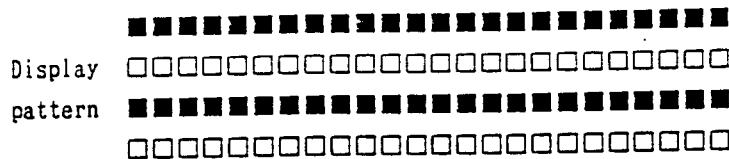
    This value is direct current.

5-3 Interface signals

○ L C D   Table 7

Pin No	Symbol	Description	Level
1	DL4	Display data signal (Lower)	H(ON), L(OFF)
2	V_{ss}	Ground potential	—
3	DL5	Display data signal (Lower)	H(ON), L(OFF)
4	YD	Scan start-up signal	"H"
5	DL6	Display data signal (Lower)	H(ON), L(OFF)
6	LP	Input data latch signal	"H"→"L"
7	DL7	Display data signal (Lower)	H(ON), L(OFF)
8	V_{ss}	Ground potential	—
9	V_{ss}	Ground potential	
10	XCK	Data input clock signal	"H"→"L"
11	DL0	Display data signal (Lower)	H(ON), L(OFF)
12	V_{CON}	Contrast adjust voltage	—
13	DL1	Display data signal (Lower)	H(ON), L(OFF)
14	V_{DD}	Power supply for logic and LCD (+5V)	—
15	V_{ss}	Ground potential	
16	V_{DD}	Power supply for logic and LCD (+5V)	—
17	DL2	Display data signal (Lower)	H(ON), L(OFF)
18	DISP	Display control signal	H(ON), L(OFF)
19	DL3	Display data signal (Lower)	H(ON), L(OFF)
20	NC	—	—
21	V_{ss}	Ground potential	—
22	DU3	Display data signal (Upper)	H(ON), L(OFF)
23	DU4	Display data signal (Upper)	H(ON), L(OFF)
24	DU2	Display data signal (Upper)	H(ON), L(OFF)
25	DU5	Display data signal (Upper)	H(ON), L(OFF)
26	DU1	Display data signal (Upper)	H(ON), L(OFF)
27	V_{ss}	Ground potential	—
28	DU0	Display data signal (Upper)	H(ON), L(OFF)
29	DU6	Display data signal (Upper)	H(ON), L(OFF)
30	V_{ss}	Ground potential	—
31	DU7	Display data signal (Upper)	H(ON), L(OFF)

○ C C F T

Pin No	Symbol	Description	Level
1	HV	High voltage lineal (from Inverter)	—
2	NC		—
3	GND	Ground line (from Inverter)	—

NOTE) Pin No. and its location are shown in Fig.10.

○ L C D

    Used   connector:DF9B-31P-1V (HIROSE)

    Mating connector:DF9B-31S-1V (HIROSE)

○ C C F T

    Used   connector:BHR-03VS-1   (JST)

    Mating connector:SM03(4.0)B-BHS or SM02(8.0)B-BHS (JST)

    Except above connector shall be out of guaranty

640×3 (RGB)
×480 dots

(1, 1) (1, 2)   COLUMN   (1, 639) (1, 340)

(2, 1) (2, 2)   (2, 639) (2, 340)

ROW

(479, 1) (479, 2)   (479, 639) (479, 340)

| R | G | B | R | G | B | | R | G | B | R | G | B |
| R | G | B | R | G | B | | R | G | B | R | G | B |

(480, 1) (480, 2)   (480, 639) (480, 340)

| R DL 7 | G DL 6 | B DL 5 | R DL 4 | G DL 3 | B DL 2 | R DL 1 | G DL 0 | B DL 7 | R DL 6 | G DL 5 | B DL 4 | R DL 3 | G DL 2 | B DL 1 | R DL 0 | | R DL 5 | G DL 4 | B DL 3 | R DL 2 | G DL 1 | B DL 0 |
| R DL 7 | G DL 6 | B DL 5 | R DL 4 | G DL 3 | B DL 2 | R DL 1 | G DL 0 | B DL 7 | R DL 6 | G DL 5 | B DL 4 | R DL 3 | G DL 2 | B DL 1 | R DL 0 | | R DL 5 | G DL 4 | B DL 3 | R DL 2 | G DL 1 | B DL 0 |

☐: Lower SEG Drivers
   Lower data (DL0～7)
▨: Upper SEG Drivers
   Upper data (DU0～7)
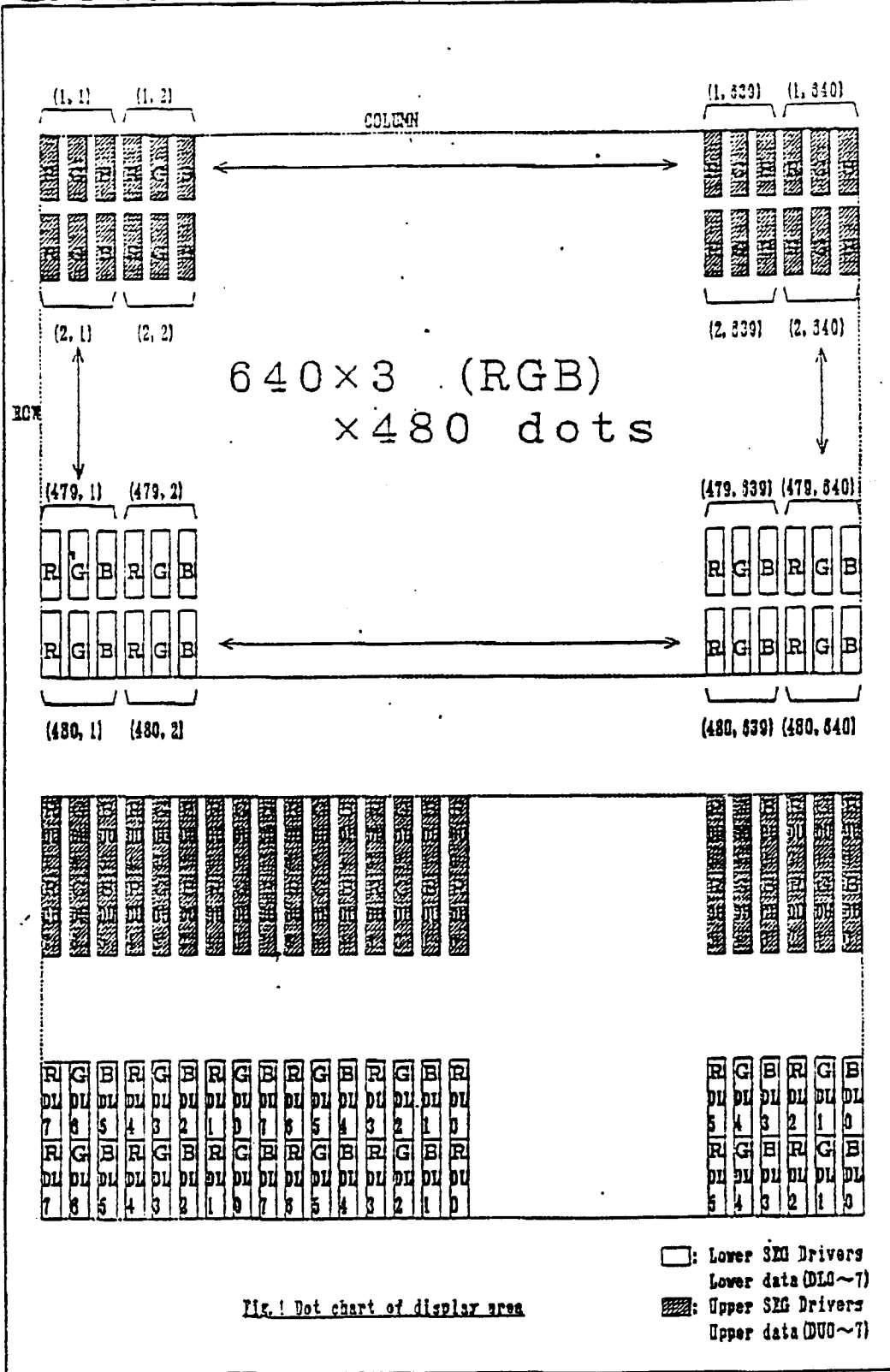
Fig. 1 Dot chart of display area

SHARP

LP×244 pulses

YD

LP

| DUO ~ DU7 | 1st line's display data | 2nd line's display data | | 244th line's display data | 1st line's display data | 2nd line's display data | |

| DLO ~ DL7 | 241th line's display data | 242th line's display data | | 484th line's display data | 241th line's display data | 242th line's display data | |

XCK × 640 × (3/8) pulses

LP

XCK

XCK

DU7	R(1,1)	B(1,3)	G(1,6)		R(1,9)	B(1,11)	G(1,14)	
DU6	G(1,1)	R(1,4)	B(1,6)		G(1,9)	R(1,12)	B(1,14)	
DU5	B(1,1)	G(1,4)	R(1,7)		B(1,9)	G(1,12)	R(1,15)	
DU4	R(1,2)	B(1,4)	G(1,7)		R(1,10)	B(1,12)	G(1,15)	
DU3	G(1,2)	R(1,5)	B(1,7)		G(1,10)	R(1,13)	B(1,15)	
DU2	B(1,2)	G(1,5)	R(1,8)		B(1,10)	G(1,13)	R(1,16)	
DU1	R(1,3)	B(1,5)	G(1,8)		R(1,11)	B(1,13)	G(1,16)	
DUO	G(1,3)	R(1,6)	B(1,8)		G(1,11)	R(1,14)	B(1,16)	

DL7	R(241,1)	B(241,3)	G(241,6)		R(241,9)	B(241,11)	G(241,14)	
DL6	G(241,1)	R(241,4)	B(241,6)		G(241,9)	R(241,12)	B(241,14)	
DL5	B(241,1)	G(241,4)	R(241,7)		B(241,9)	G(241,12)	R(241,15)	
DL4	R(241,2)	B(241,4)	G(241,7)		R(241,10)	B(241,12)	G(241,15)	
DL3	G(241,2)	R(241,5)	B(241,7)		G(241,10)	R(241,13)	B(241,15)	
DL2	B(241,2)	G(241,5)	R(241,8)		B(241,10)	G(241,13)	R(241,16)	
DL1	R(241,3)	B(241,5)	G(241,8)		R(241,11)	B(241,13)	G(241,16)	
DLO	G(241,3)	R(241,6)	B(241,8)		G(241,11)	R(241,14)	B(241,16)	

Fig.2 Data input timing chart

Table 8 Interface timing ratings

Item	Symbol	MIN.	TYP.	MAX.	Unit
Frame cycle *1	tFRM	8.33		16.94	ms
YD signal "H" level set up time	tHYS	100			ns
"H" level hold time	tHYH	100			ns
"L" level set up time	tLYS	100			ns
"L" level hold time	tLYH	40			ns
LP signal "H" level pulse width	tWLPH	200			ns
XCK signal clock cycle	tCK	82			ns
"H" level clock width	tWCKH	30			ns
"L" level clock width	tWCKL	30			ns
Data set up time	tDS	30			ns
hold time	tDH	30			ns
LP↑ allowance time from XCK↓	tLS	200			ns
XCK↑ allowance time from LP↓	tLH	200			ns
Input signal rise/fall time	tr,tf			13	ns
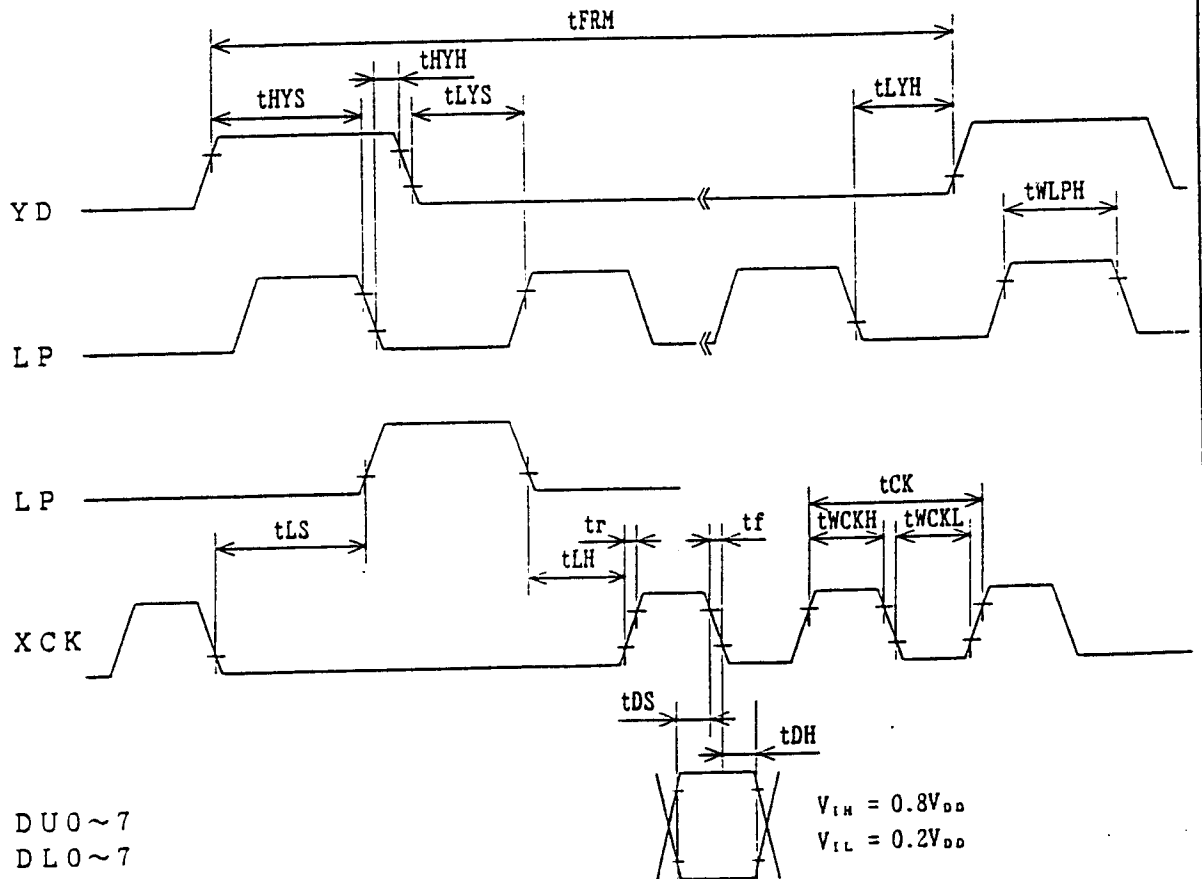
Fig.3 Interface timing chart

*1 LCD unit functions at the minimum frame cycle of 8.33 ms(Maximum frame frequency of
120 Hz).
Owing to the characteristics of LCD unit,˜shadowing˜ will become more eminent as
frame frequency goes up,˜whle flicker will be reduced.

According to our experiments,frame cycle of 12.8 ms Min. or frame frequency of 78 Hz
Max. will demonstrate optimum display quality in terms of flicker and ˜shadowing˜.
But since judgement of display quality is subjective and display quality such as
˜shadowing˜ is patturn dependent,it is recommended that decision of frame frequency,
to which power consumption of the LCD unit is propotional,be made based on your
own through testing on the LCD unit with every possible patterns displayed on it.

※ The intervals of one LP fall and the next must be always the same, and LPs must be
input continuously.
The interval must be 70μs Max.

6. Unit Driving Method

6.1 Circuit configuration

Fig.10 shows the block diagram of the Unit's circuitry.

6.2 Display Face Configuration

The display consists of 640x3 (R,G,B)x480 dots as shown in Fig.1.

The interface is single panel with double drive to be driven at 1/244 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 160 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (640x3 R,G,B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal(XCK)

When input of one row (640 x 3,R,G,B dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP). Then, the corresponding drive signals will be transmitted to the 640 x 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 640x3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 244th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Simultaneously the same scanning sequence occur at the lower panel.

Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display unit goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system of transferring 8 bit parallel data through the 8 lines of shift registers.
Thanks to this system the power consumption of the display unit is minimized.

In this circuit configuration, 8 bit display data shall input to data input pins of DU0~7 and DL0~7.

Furthermore, the display unit has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 160 dot (20XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. This process is followed simultaneously both at the top and bottom column drivers LSI's.

Thus data input will be made through 8 bit bus line sequentially from the left end of the display face.

Since this display unit contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 8.

7.Optical Characteristics

$Ta = 25 °C, V_{DD} = 5.0 V, Vcon-V_{SS} = Vmax$

Table 9

Following spec are based upon the electrical measuring conditions,
on which the contrast of perpendicular direction ($\theta x = \theta y = 0$ °)will be MAX.

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	$Co > 5.0$	$\theta y = 0$ °	-30	-	30	dgr.	Note1)
		θy		$\theta x = 0$ °	-15	-	25	dgr.	
Contrast ratio		Co	$\theta x = \theta y = 0$ °		15	30	-		Note2)
Response time	Rise	τr	$\theta x = \theta y = 0$ °		-	220	300	ms	Note3)
	Decay	τd	$\theta x = \theta y = 0$ °		-	80	100	ms	
Unit chromaticity	White	x	$\theta x = \theta y = 0$ °		-	0.275	-	—	
		y	$\theta x = \theta y = 0$ °		-	0.320	-	—	

Note 1) The viewing angle range is defined as shown Fig.4.

Note 2) Contrast ratio is defined as follows:

$$Co = \frac{Luminance(brightness) \; all \; pixels \; \text{"White"} \; at \; Vmax}{Luminance(brightness) \; all \; pixels \; \text{"dark"} \; at \; Vmax}$$

Vmax is defined in Fig.6.
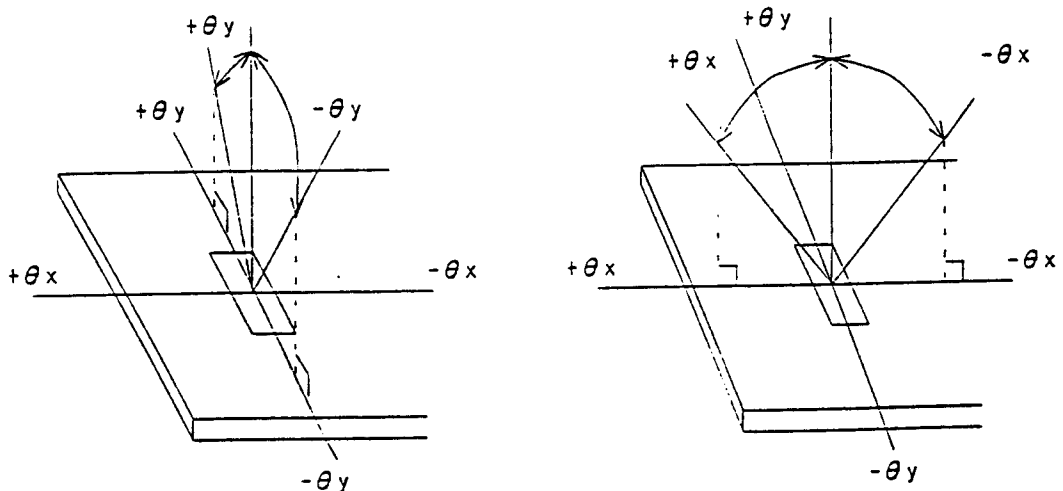
Fig.4　Definition of Viewing Angle

Note 3) The response characteristics of photo-detector output are measured as
shown in Fig.7,assuming that input signals are applied so as to select
and deselect the dots to be measured, in the optical characteristics
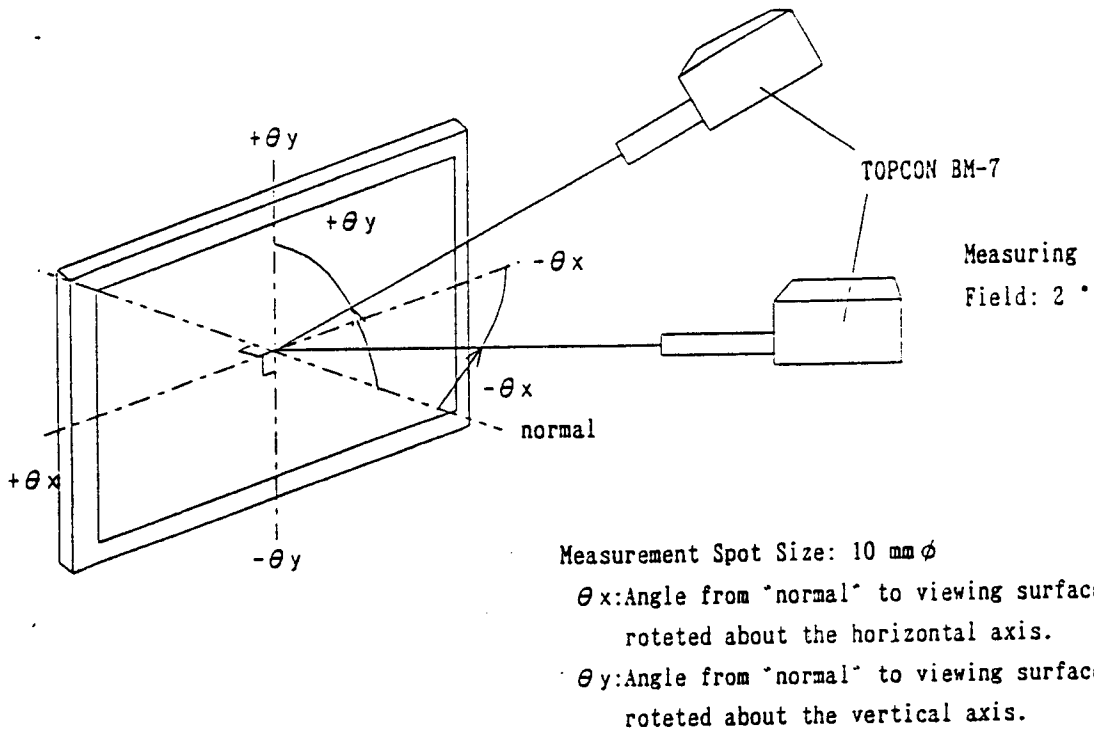test method shown in Fig.8.

TOPCON BM-7

Measuring
Field: 2 °

Measurement Spot Size: 10 mm ϕ
θ x:Angle from "normal" to viewing surface
roteted about the horizontal axis.
θ y:Angle from "normal" to viewing surface
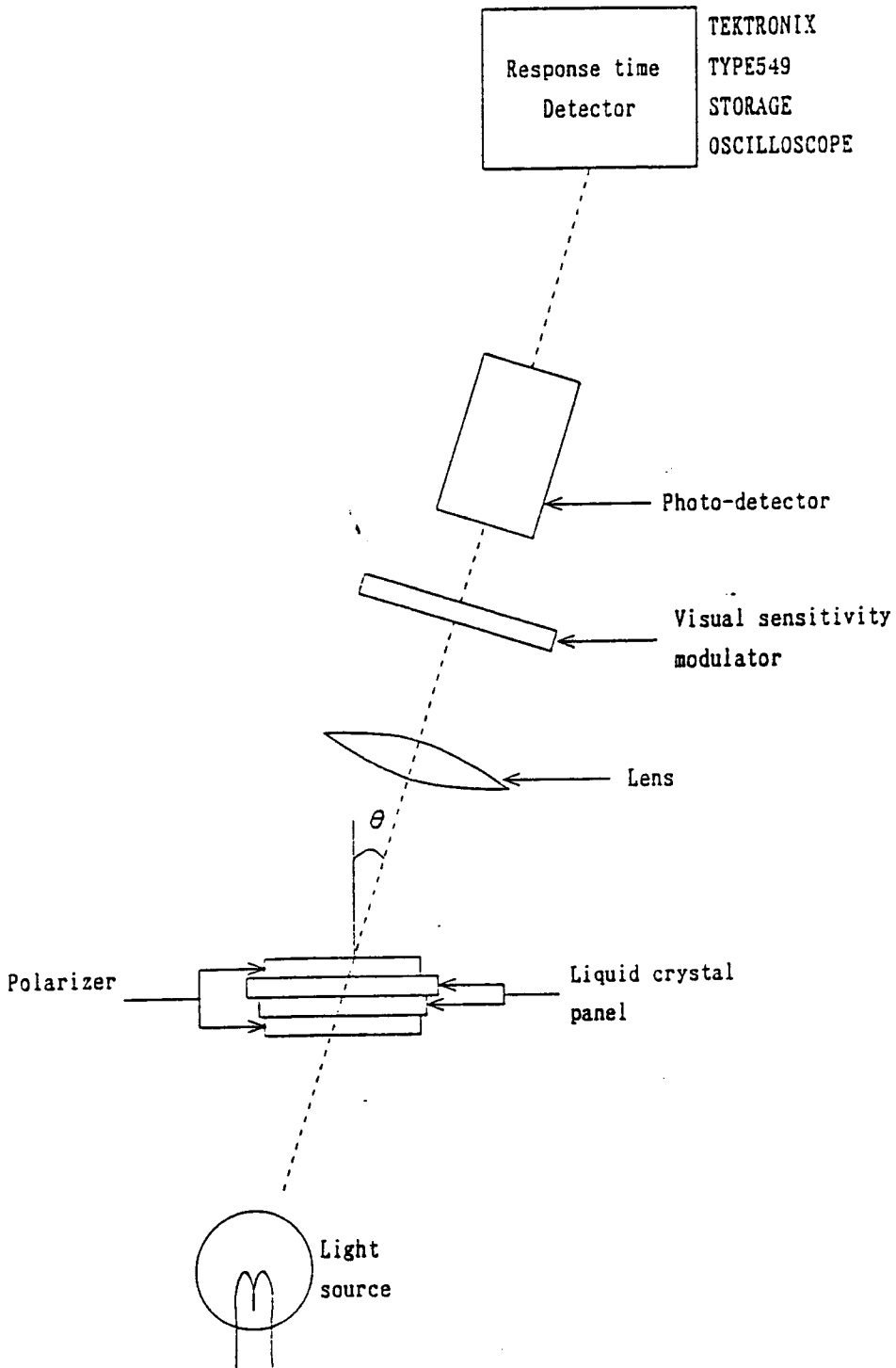roteted about the vertical axis.

Fig. 5 Optical Characteristics Test Method I

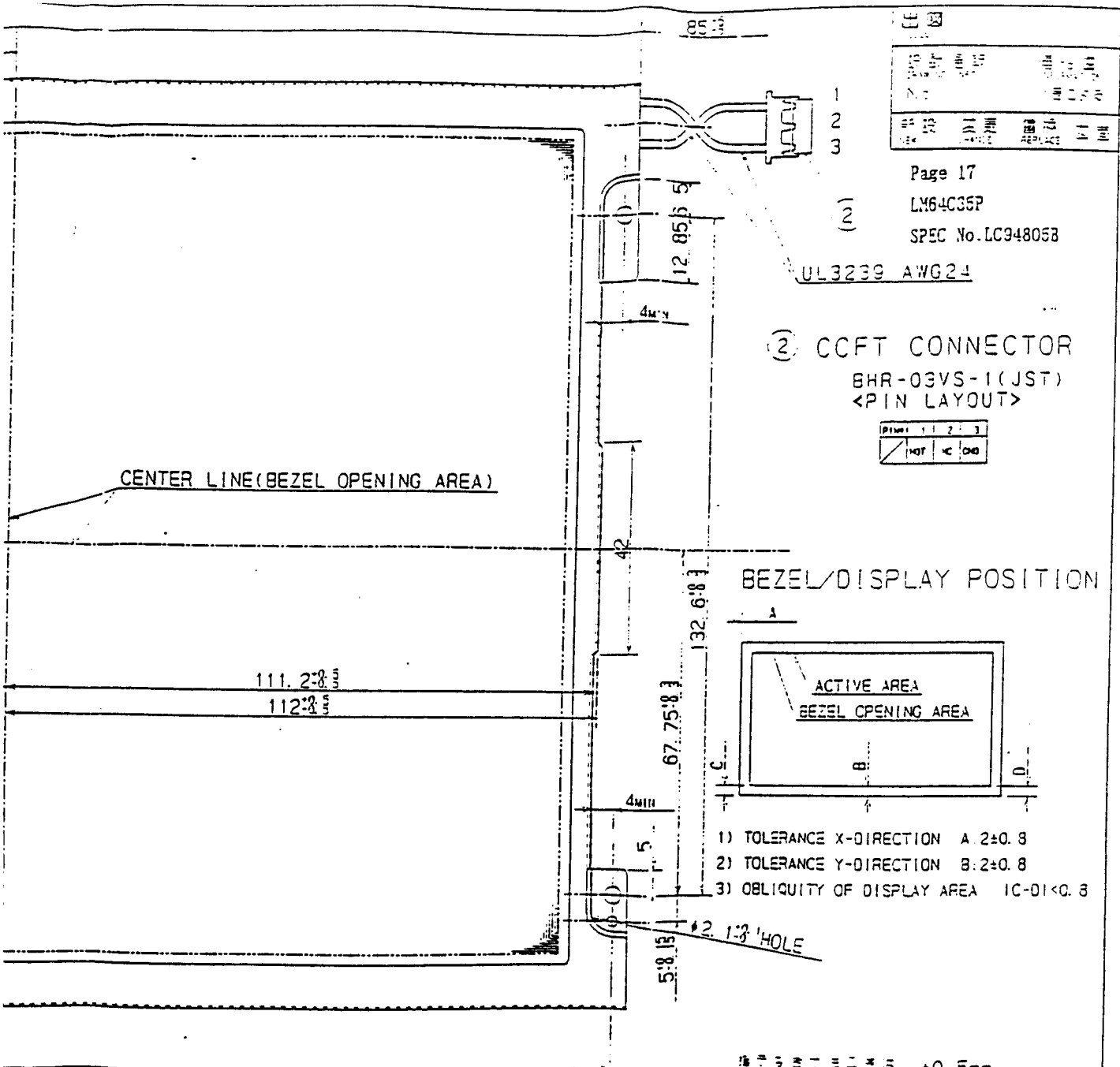
Fig. 6 Definition of Vmax

Response time Detector — TEKTRONIX TYPE549 STORAGE OSCILLOSCOPE

Photo-detector

Visual sensitivity modulator

Lens

θ

Polarizer

Liquid crystal panel

Light source

Fig.7 Optical Characteristics Test Method II

[Drive waveform]

1/244 Duty Ratio

driving

voltage

Non-select
—— waveform —— ——← select waveform ——→←—

Non-select
—— waveform ——

[Response waveform]

Photo-
detector
output

100 % 90 %

10 %

τr τd

τr: Rise time
τd: Decay time
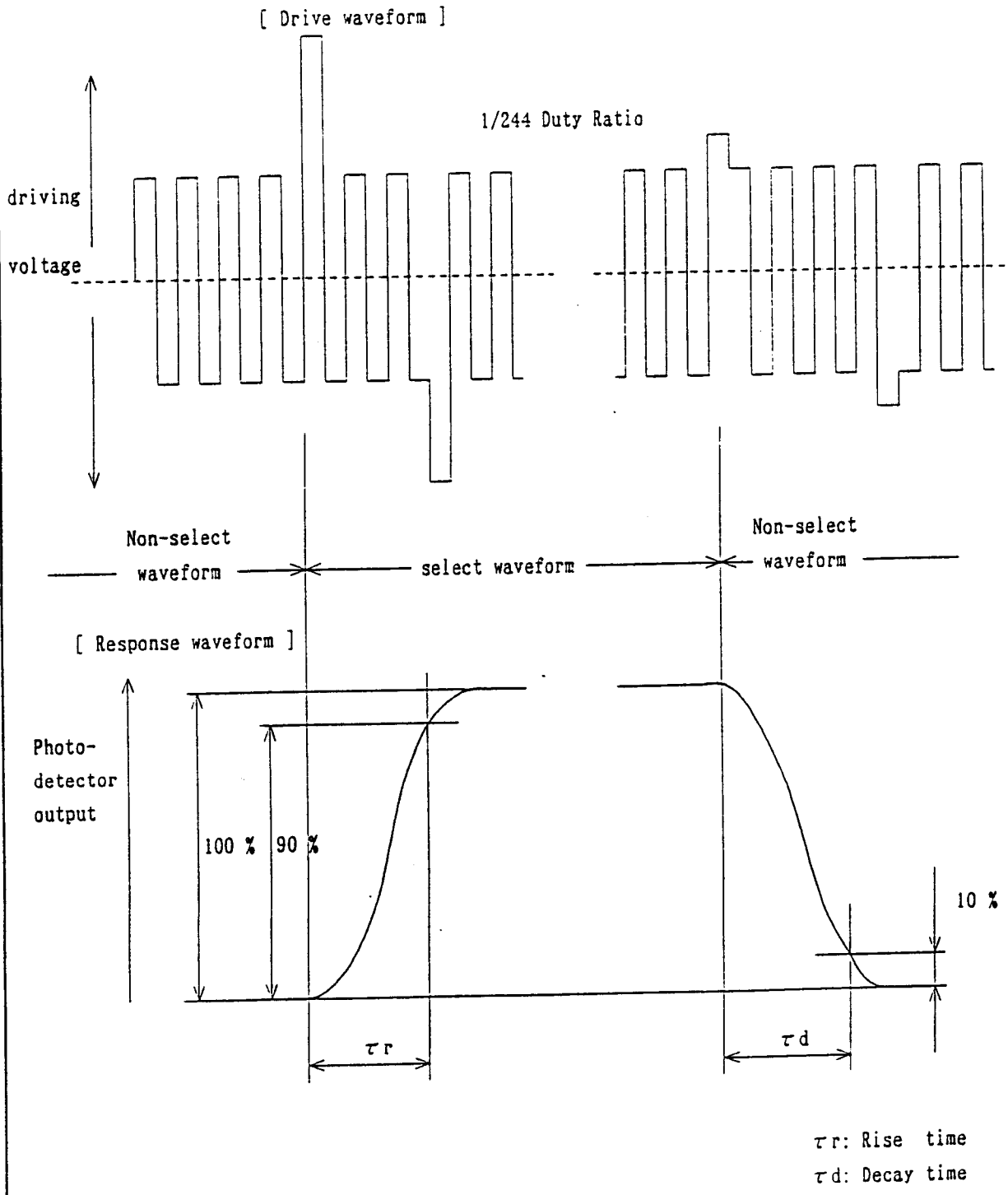
Fig.8 Definition of Response Time

DUO~DU7
DLO~DL7 CMOS
XCK   Buffer
         I.C.
LP

YD
DISP   DISP

SEG Drivers (Upper)

Sequence
Control
Circuit

C
O
M

D
r
i
v
e
r
s

R G B R

*1 MG

X X X X

640×3(RGB)×480
LCD PANEL

R G B R

SEG Drivers (Lower)

Inverter - - - - - - CCFT
                       B/L

*2 BG

VEE

V_{DD}   DC/DC
V_{ss}   Converter
Vcon

*1 MG: M GENERATOR CIRCUIT
*2 BG: BIAS GENERATOR & PROTECTION CIRCUIT
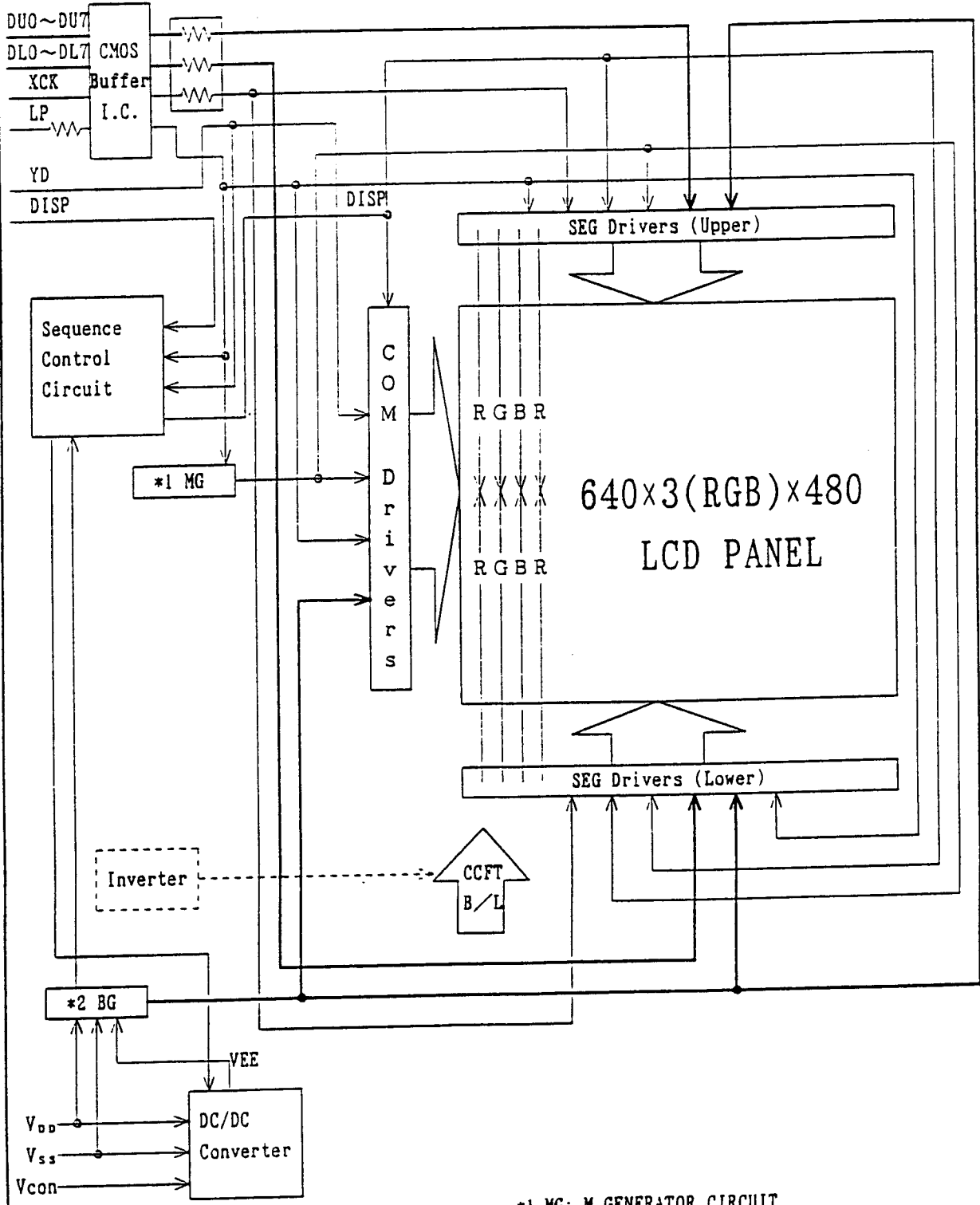
<u>Fig.9 Circuit block diagram</u>

242.5

123.5

4-3.4±0.15HOLE

4MIN

4mm

ACTIVE AREA
211.175×158.375

BEZEL OPENING AREA
215.2±0.3×162.4±0.3

4-R4

31   30

1   2

(-1)

2.5

118

170.4

166.6

89.7

84.75

5.55

2.1

2-3.15

7.6

4-R0.5

4MIN

118.5

234

11.5MAX

5.6

2.5

Excluded the allowance of deformation

(1) INTERFACE CONNECTOR
DF9B-31P-1V(HIROSE)
<PIN LAYOUT>

Pin#	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	GND	GND	GND	RS	GND	LP	GND	GND	GND	RC	GND/VCOM	GND	VCC
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	VCC	CLK/DISP	GND	XK	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

LM64C35P

SPEC No. LC94805B

UL3239 AWG24

② CCFT CONNECTOR

BHR-03VS-1(JST)

<PIN LAYOUT>

Pin	1	2	3
	HOT	IC	GND

CENTER LINE(BEZEL OPENING AREA)

BEZEL/DISPLAY POSITION

ACTIVE AREA

BEZEL OPENING AREA

1) TOLERANCE X-DIRECTION   A.2±0.8

2) TOLERANCE Y-DIRECTION   B.2±0.8

3) OBLIQUITY OF DISPLAY AREA   IC-DI<0.8

111.2

112

4MIN

φ2.1 HOLE

UNSPECIFIED ±0.5mm

		LM64C35P			LCD UNIT OUTLINE DIMENSIONS
					640×R·G·B×480DOTS 1/240 DUTY
			SHARP CORPORATION		1994 2 23
			シャープ株式会社		CD101 4-73

Fig.10 OUTLINE DIMENSIONS

8.Characteristics of Backlight

      The ratings are given on condition that the following conditions are satisfied.

1) Rating (Note)

Parameter	Min	Typ	Max	Unit
Brightness	50	70	—	cd/m²

2) Measurement circuit: CXA-M10L (TDK) (at IL=5.4 mArms)

3) Measurement equipment: BM-7 (TOPCON Corporation)

4) Measurement conditions

    4-1 Measurement circuit voltage: DC=9.6 V, at primary side

    4-2 LCD: All digits WHITE, V_{DD}= 5 V,Vcon-Vss=Vmax,DU0~7="H"(WHITE),DL0~7="H"(WHITE)

    4-3 Ambient temperature: 25 ℃

        Measurement shall be executed 30 minutes after turning on.

5) Used lamp: HMBS26D10W217C/X HARISON ELECTRIC CO.,LTD.　: 1 pc

  ⚠ 5-1 Rating

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	-	480	-	Vrms	—
Lamp current	I_L	3.8	5.4	6.0	mArms	(*1)
Lamp power consumption	P_L	-	2.6	-	W	(*2)
Lamp frequency	F_L	20	-	50	kHz	—
Kick-off voltage	V_S	-	-	900	Vrms	Ta=25℃
		-	-	1100	Vrms	Ta=0℃ (*3)
Lamp life time	L_L	10000	-	-	h	—

            Within no conductor closed. (CCFT only)

    (*1) It is recommended that IL be not more than 5.4 mArms so that heat
           radiation of CCFT backlight may least affect the display quality.

    (*2) Power consumption excluded inverter loss.

    (*3) The circuit voltage(VS) of the inverter should be designed to have
           some margin(reference value:1 450 VrmsMIN),because VS may be
           increased due to the leak current in case of the LCD unit.

    5-2 Operating life

        The operating life time is 10 000 hours or more at 5.4 mA.

        (Operating life with CXA-M10L-L or equivalent.)

        The inverter should meet the following conditions to keep the specified
        life time of used lamp;
        -Sine, symmetric waveform without spike in positive and negative.
        -Output frequency range: 20 KHz~50 KHz
        Make sure the operating conditions by executing the burn-in enough time.

The operating life time is defined as having ended when any of
the following conditions occur; 25±1 °C
-When the voltage required for initial discharge has reached
110 % of the initial value
-When the illuminence or quantity of light has decreased to
50 % of the initial value

(NOTE) Rating are defined as the average brightness inside the viewing
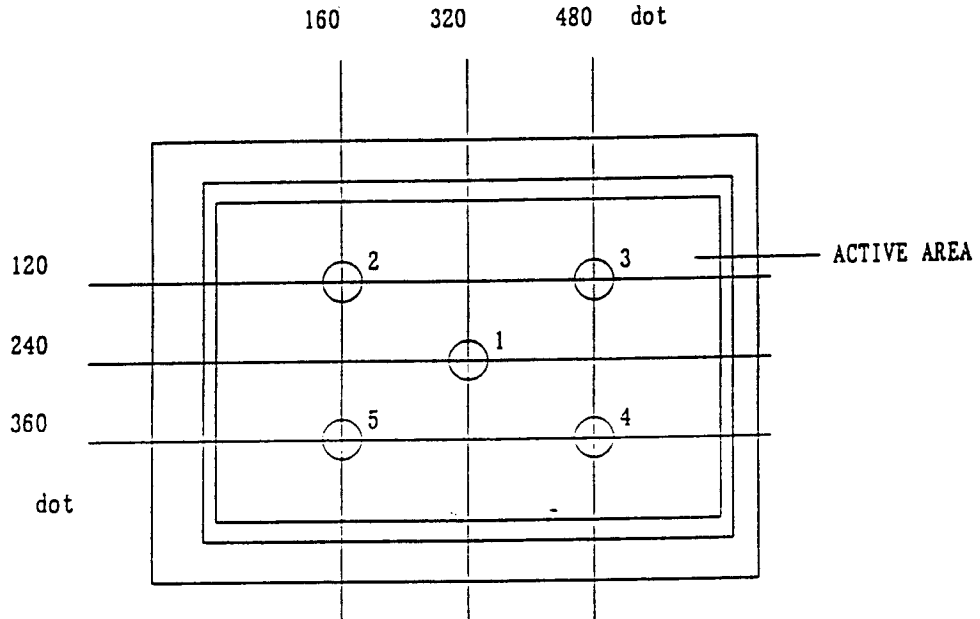area specified in Fig.11.

Fig.11 Measureing points (1~5)

9. Precautions

   1) Industrial (Mechanical)design of the product in which this LCD unit will be
      incorporated must be made that the viewing angle characteristics of the
      LCD may be optimized.
      This unit's viewing angle is illustrated in Fig.12.
          θy MIN < viewing angle < θy MAX   ⚠
          (For the specific values of $\theta ymin$. $\theta ymax$. refer to the table 9.)
      Please consider the optimum viewing conditions according to the purpose
      when installing the unit.
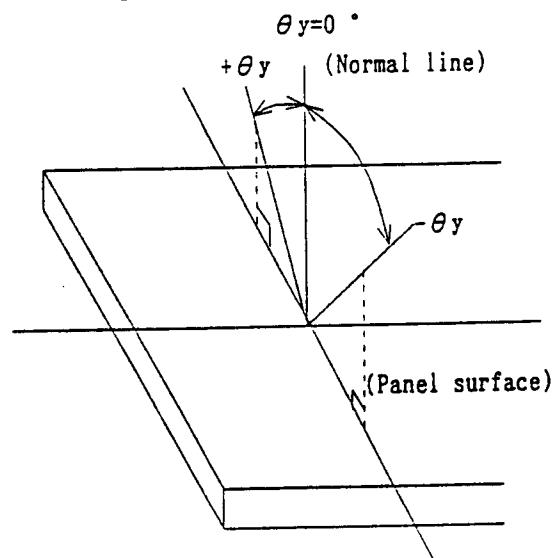
Fig.12 Dot matrix LCD viewing angle

   2) This unit is installed using mounting holes metal PBC or bezel.
      When installing the unit, pay attention and handle carefully not to allow any
      undue stress such as twist or bend.
      A transparent acrylic resin board or other type of protective panel should be
      attached to the front of the unit to protect the polarizer, LCD cells,etc.

3) Since the front polarizer is easily damaged. Please pay attention not to scratch on its face.

4) If the surface of the LCD cells needs to be cleaned, wipe it swiftly with cotton or other soft cloth. If still not completely clear, blow on its and wipe.

5) Water droplets, etc, must be wiped off immediately since they may cause color changes, staining, etc, if remained for a long time.

6) Since LCD is made of glass plates, dropping the unit or banging it against hard objects may cause cracking or fragmentation.

7) CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro static charge, by earthing human body, etc. Take the following measures, to protect the unit from the electric discharge via mounting tabs from the main system the electrified with static electricity.
   (1) Earth the metallic case of the main system (contact of the unit and main system).
   (2) Insulate the unit and main system by attaching insulating washers made of bakelite or nylon,etc.

8) The unit should be driven according to the specified ratings to avoid malfunction of parmanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Especially the power ON/OFF sequence shown on next page is strongly recommended to avoid latch-up of drive LSIs and application of DC voltage to LCD panel.

9) Since leakage current, which may be caused by routing of CCFT cables,etc., may affect the brightness of the display, the inverter has to be designed taking the leakage current into consideration. Thorough evaluation of the LCD unit/inverter built into its host equipment shall be conducted, therefore, to ensure the specified brightness.

10) Avoid to expose the unit to the direct sun-light, strong ultraviolet light, etc. for a long time.

11) If stored at temperatures below specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating. the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state. As for as possible always store at normal room temperature.

12) Disassembling the LCD unit can cause permanent damege and should be strictly avoided.

⚠4

13)How to insert interface connector

When the interface connector is inserted, it should be parallel to the connector of LCD module and it should be inserted horizontally.
When the connector is attempted to be fixed to LCD connector, it should be inserted properly in order not to create a gap as shown "A".
Please insert the connector as both edge is placed to the connect position of LCD connector.

LCD connector

LCD connector

LCD connector
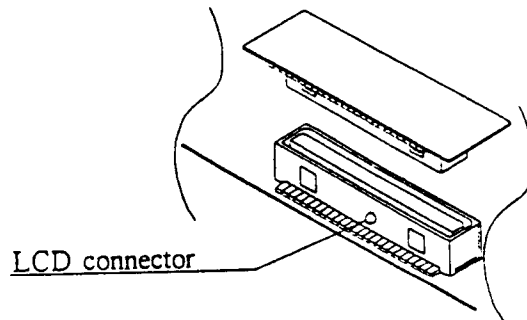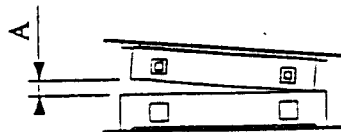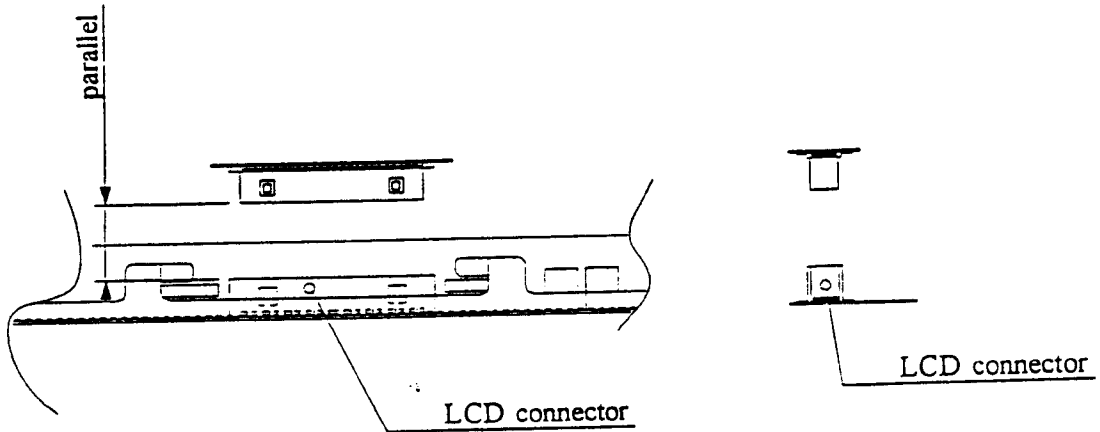
Supplt voltage sequence condition
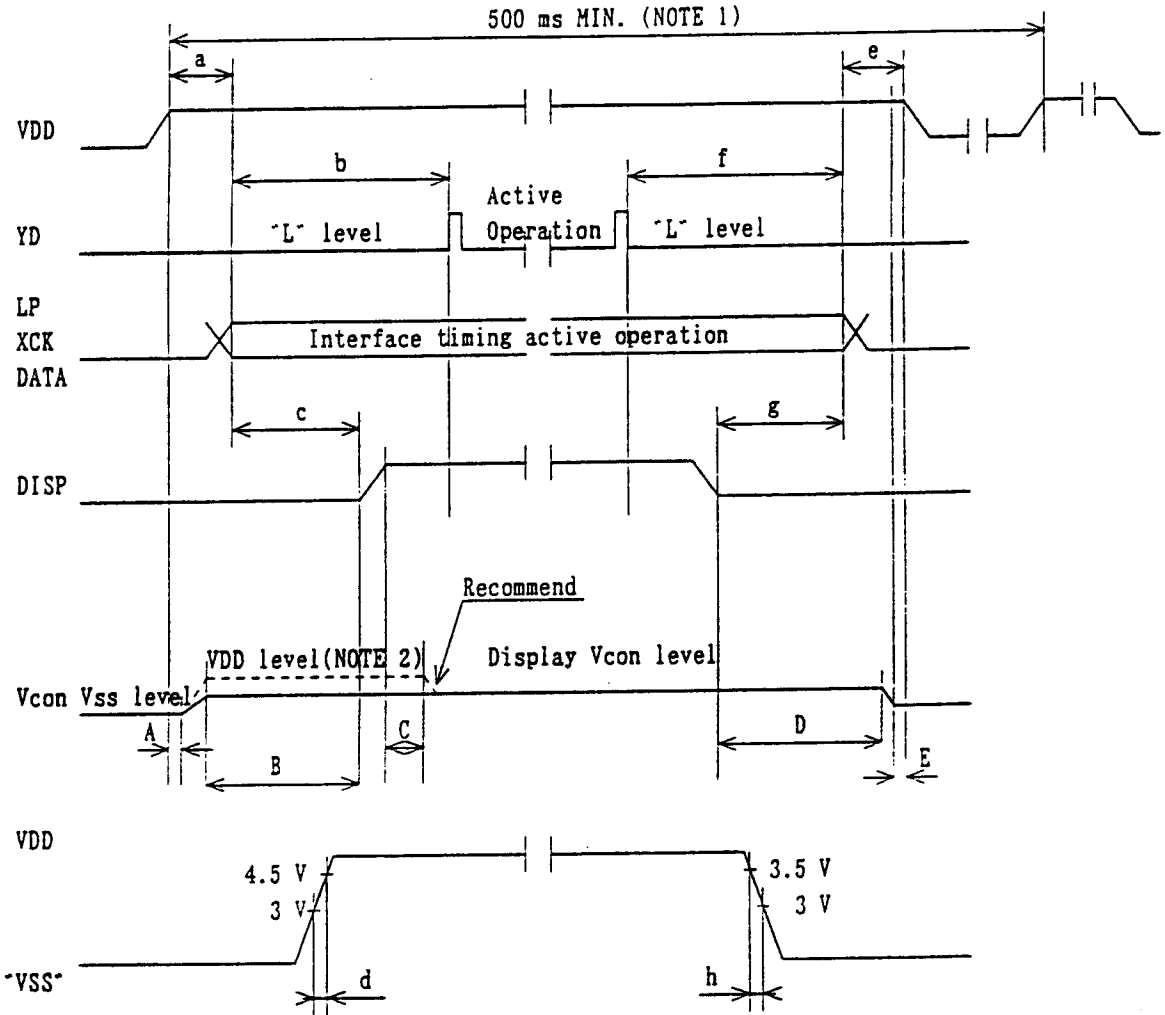
500 ms MIN. (NOTE 1)

	POWER ON	
SYMBOL	Allowable value	
a	0 ms MIN.	1 s MAX.
b	0 ms MIN.	1 s MAX.
c	LP×250 MIN.	1 s MAX.
d	—	25 ms MAX.
A	0 ms MIN.	—
B	0 ms MIN.	—
C	60 ms MIN.(NOTE 2) Recommend	

	POWER OFF	
SYMBOL	Allowable value	
e	0 ms MIN.	1 s MAX.
f	0 ms MIN.	—
g	0 ms MIN.	1 s MAX.
h	1 ms MIN.	—
D	0 ms MIN.	—
E	0 ms MIN.	—

(NOTE 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

(NOTE 2) In order to reduce the rush current, It is recommended that "Vcon" to be set to "VDD" level after power on. C(60 ms MIN.) is recommended.
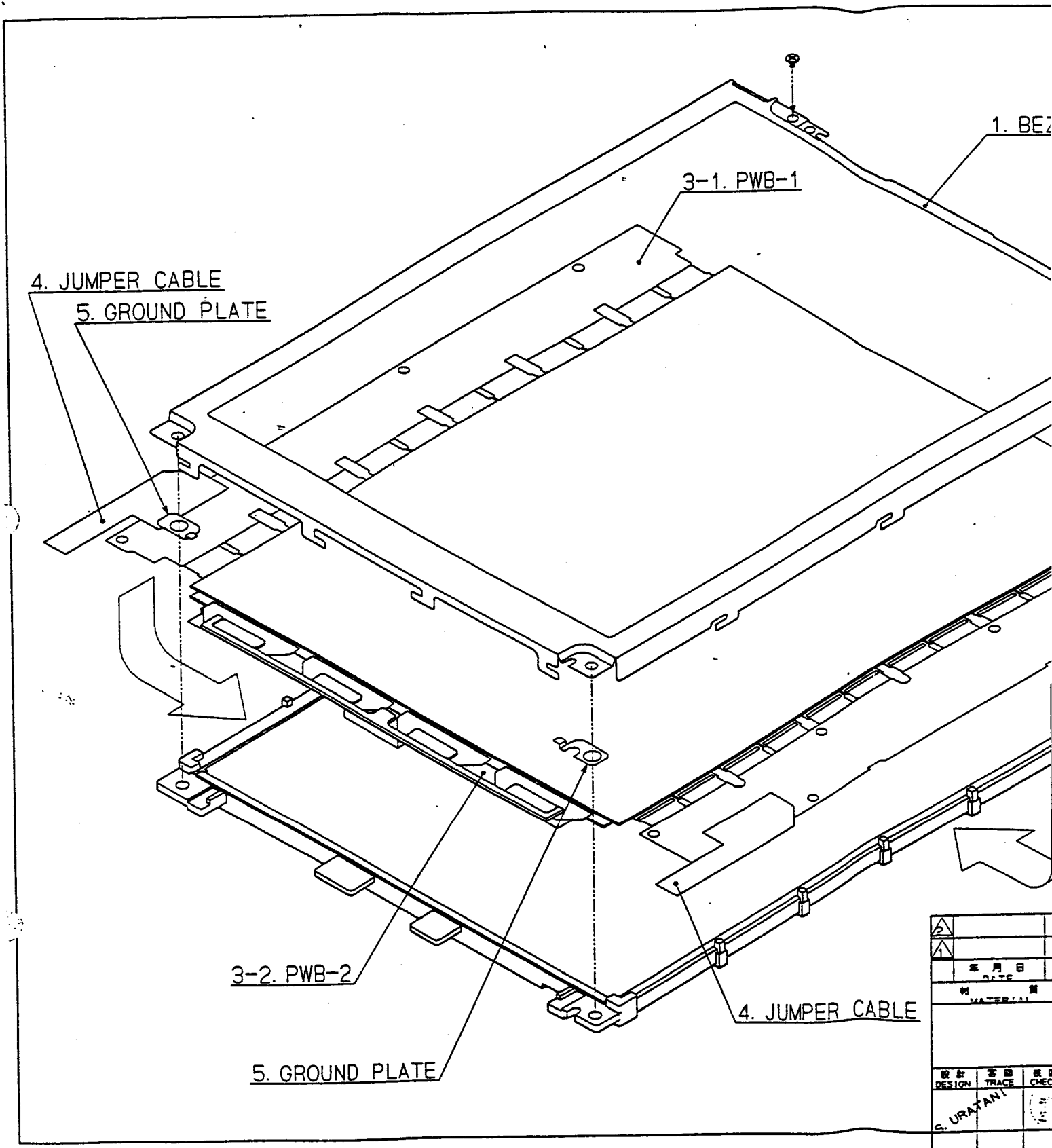
9. Applicable inspection standard
    The LCD unit shall meet the following inspection standard
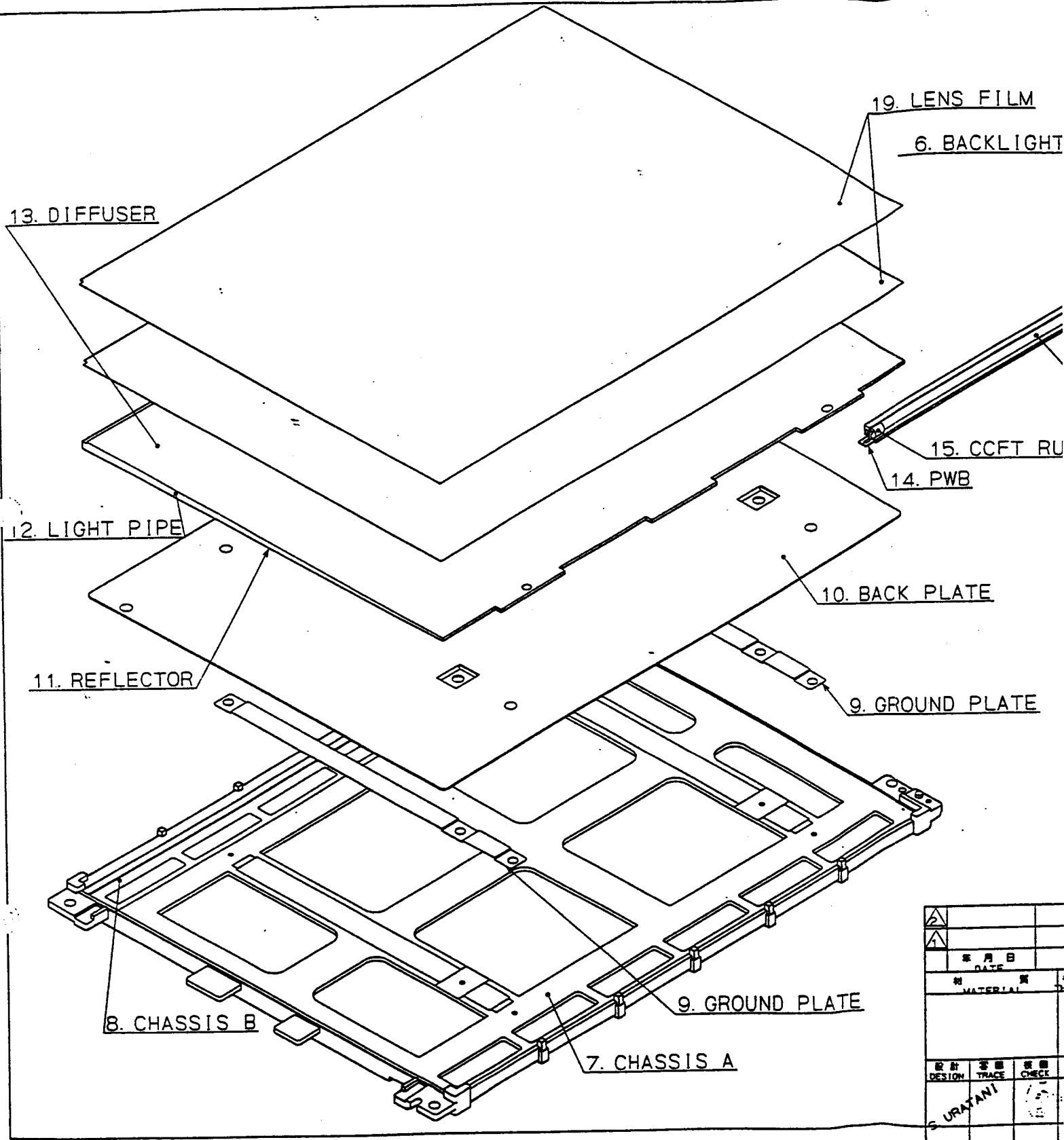   :S-U-014

10. This specification describes display quality in case of no gray scale.
    Since display quality can be affected by gray scale methods, display quality
    shall be carefully evaluated for the usability of the LCD UNIT in case gray
    scale is displayed on the LCD UNIT.

WARNING
    DON'T USE ANY MATERIALS WHICH EMIT FOLLOWING GAS FROM EPOXY RESIN (AMINES'
    HARDENER) AND SILICONE ADHESIVE AGENT (DEALCOHOL OR DEOXYM) TO PREVENT CHANGE
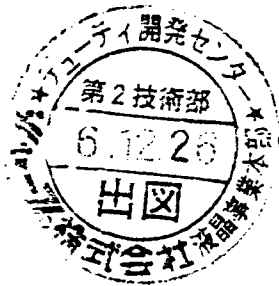   POLORIZER COLOR OWING TO GAS.

1. BE[...]

3-1. PWB-1

4. JUMPER CABLE
5. GROUND PLATE

3-2. PWB-2

4. JUMPER CABLE

5. GROUND PLATE

年 月 日
DATE
材 質
MATERIAL

設計
DESIGN
製図
TRACE
検[...]
CHE[...]

S. URATANI

19. LENS FILM

6. BACKLIGHT

13. DIFFUSER

15. CCFT RU

14. PWB

12. LIGHT PIPE

10. BACK PLATE

11. REFLECTOR

9. GROUND PLATE

8. CHASSIS B

9. GROUND PLATE

7. CHASSIS A

年 月 日
DATE

材 質
MATERIAL

設 計
DESIGN

零 図
TRACE

検 図
CHECK

S. URATANI

正 図
ISSUE
設計通報　運名書
DRAWING INFO.　INFORMATION
No. (　　　)号による
新設・変更・置換 図面
NEW　CHANGE　REPLACE

1. BEZEL

-1. PWB-1

2. LCD PANEL

3-1. PWB-1

4. JUMPER CABLE

掲示開き寸法公差は　　　とする
UNSPECIFIED TOL. TO BE

					LM64C351	名　車	Materials and component
					LM64C35P	NAME	Parts list Fig. 1
年 月 日 DATE	改 定 記 事 RIVISE		図 No	担当 PREPA	適用 MODEL		
材 質 MATERIAL	板厚 THIYNESS	仕 上 FINSH		尺度 SCALE		記　号 SYMBOL	
						部品コード PARTS CODE	
設計 DESIGN	零図 TRACE	成図 CHECK	成図 CHECK	承認 APPROVE	SHARP CORPORATION	作成日付 DATE	1994. 9. 30.
S. URATANI					シャープ株式会社 液晶 (基本) 発行部門 デューティ開発センター第2枚術部	図　書 DRAWING. No	UL64C35P6010

18. CCFT CONNECTOR

19. LENS FILM

6. BACKLIGHT HOLDER

17. CCFT WIRE

15. CCFT RUBBERCUP

16. CCFT LAMP

15. CCFT RUBBERCUP

14. PWB

10. BACK PLATE

9. GROUND PLATE

ROUND PLATE

A

第2技術部
6. 2
出図

			LM64C351	名 称	Materials and component
			LM64C35P	NAME	Parts list Fig. 2
年 月 日 DATE	改 定 記 事 REVISE	図面 No	担当 PREPA	適用 機種 MODEL	記 号 SYMBOL	
材 質 MATERIAL	板 厚 THICKNESS	仕 上 FINISH	尺度 SCALE		部品コード PARTS CODE	
設計 DESIGN	零図 TRACE	検図 CHECK	検図 CHECK	承認 APPROVE	SHARP CORPORATION	作成日付 DATE	1994. 9. 30.
S. URATANI					シャープ株式会社 液晶（事本） 発行部門 デューティ開発センター第2技術部	図 番 DRAWING No.	UL64C35P6020

UNSPECIFIED TOL TO BE とする

Fig.10 OUTLINE DIMENSIONS

Page 17
LM64C35P
SPEC No.LC948058

(2) CCFT CONNECTOR
BHR-03VS-1(JST)
<PIN LAYOUT>

UL3239 AWG21

BEZEL/DISPLAY POSITION

ACTIVE AREA
BEZEL OPENING AREA

1) TOLERANCE X-DIRECTION A 2±0.8
2) TOLERANCE Y-DIRECTION B 2±0.8
3) OBLIQUITY OF DISPLAY AREA IC-01<0.8

CENTER LINE(BEZEL OPENING AREA)

ACTIVE AREA
211.175×158.375
BEZEL OPENING AREA
215.2±0.3×162.4±0.3

4-R0.5

(1) INTERFACE CONNECTOR
DF9B-31P-1V(HIROSE)
<PIN LAYOUT>

LCD UNIT OUTLINE
DIMENSIONS

LM64C35P

640×P.G 5×480DOTS
1/240 DUTY

SHARP CORPORATION

1994.   2. 28